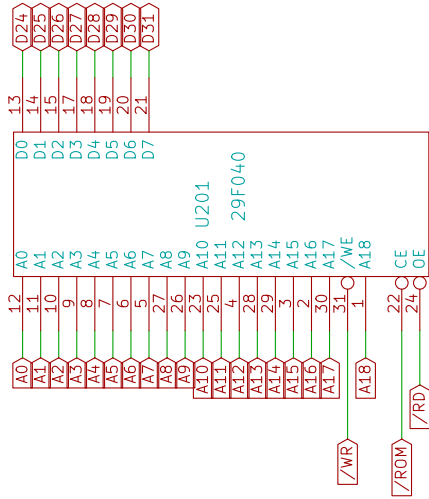
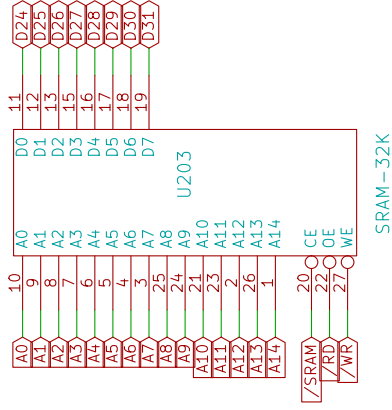


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**N8VEM Users' Group**  
 File: KISS68030.sch  
 Sheet: /  
**Title: KISS MC68030 16/32/64Mb**  
 Size: A **Date: 21 jun 2015**  
 KiCad E.D.A.



FLASH MEMORY (ROM)



512K SRAM DELETED !

(BUT ONLY THE SKINNY DIP FITS)

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**NOVEM Users' Group**

File: SRAM-ROM.sch

Sheet: /SRAM & ROM/

Title: KISS MC68030 16/32/64Mb

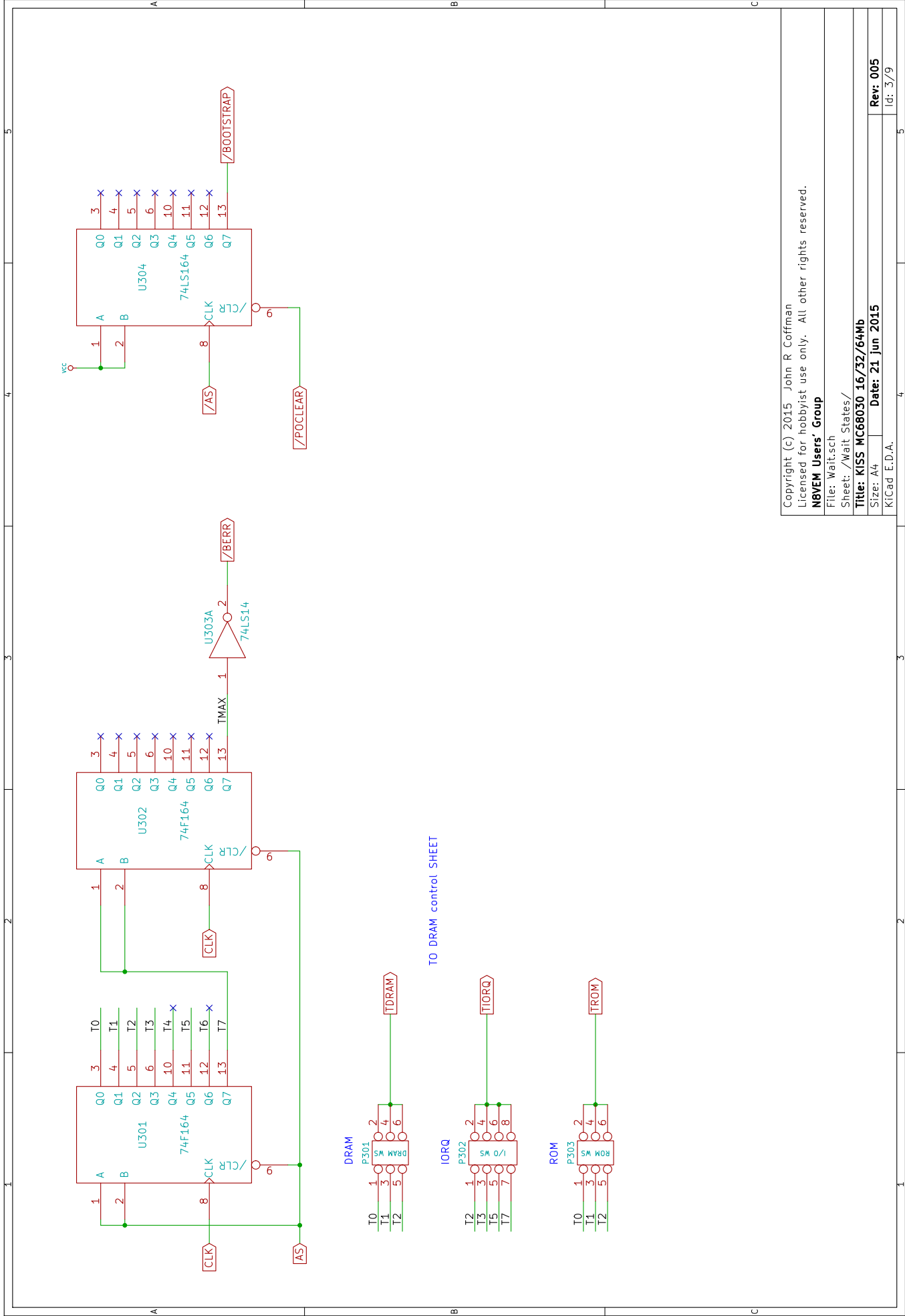
Size: A4

Date: 21 Jun 2015

KiCad E.D.A.

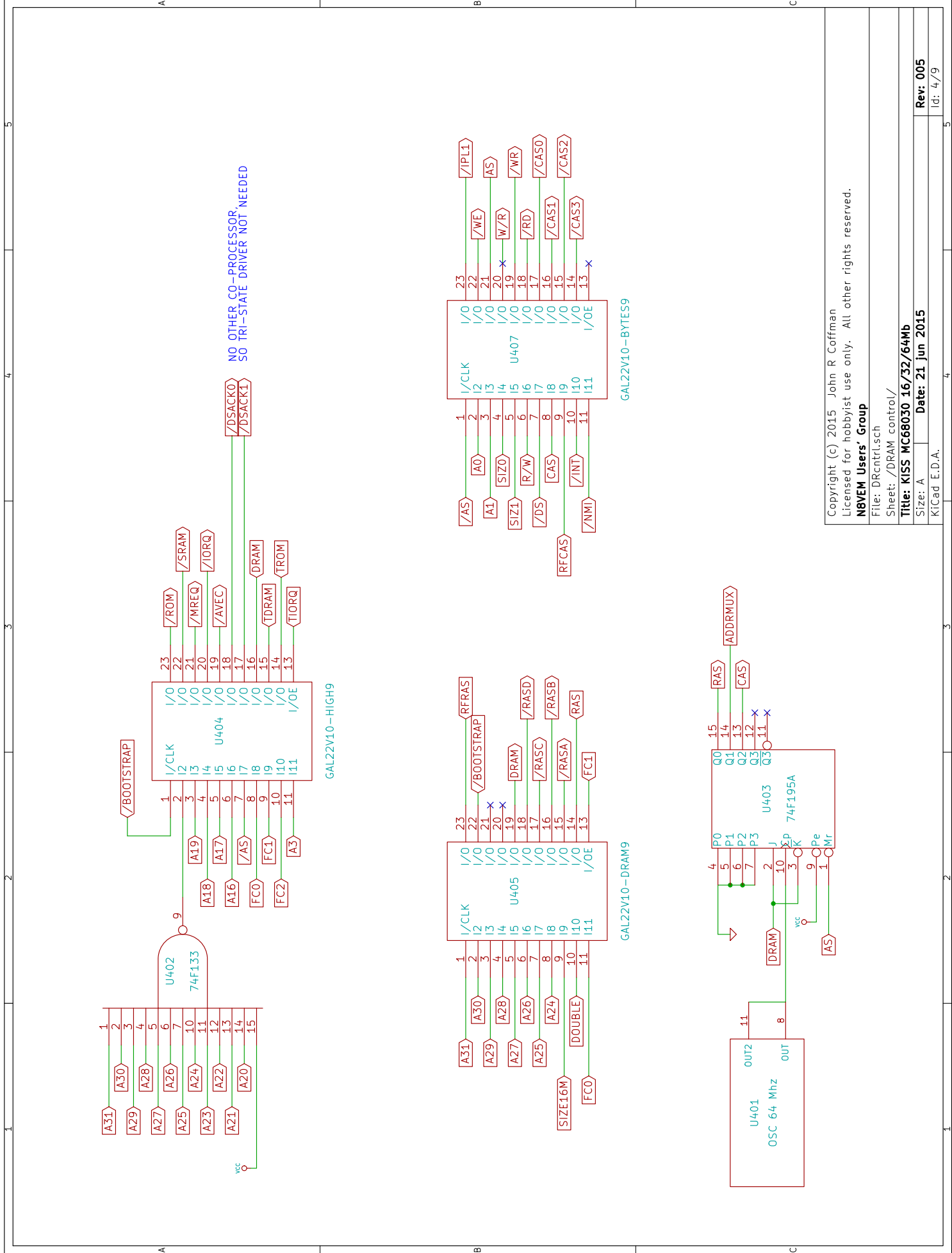
Rev: 005

Id: 2/9



TO DRAM control SHEET

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**NOVEM Users' Group**  
 File: Wait.sch  
 Sheet: /Wait States/  
**Title: KISS MC68030 16/32/64Mb**  
 Size: A4  
 Date: 21 Jun 2015  
 KiCad E.D.A. Rev: 005  
 Id: 3/9



NO OTHER CO-PROCESSOR,  
SO TRI-STATE DRIVER NOT NEEDED

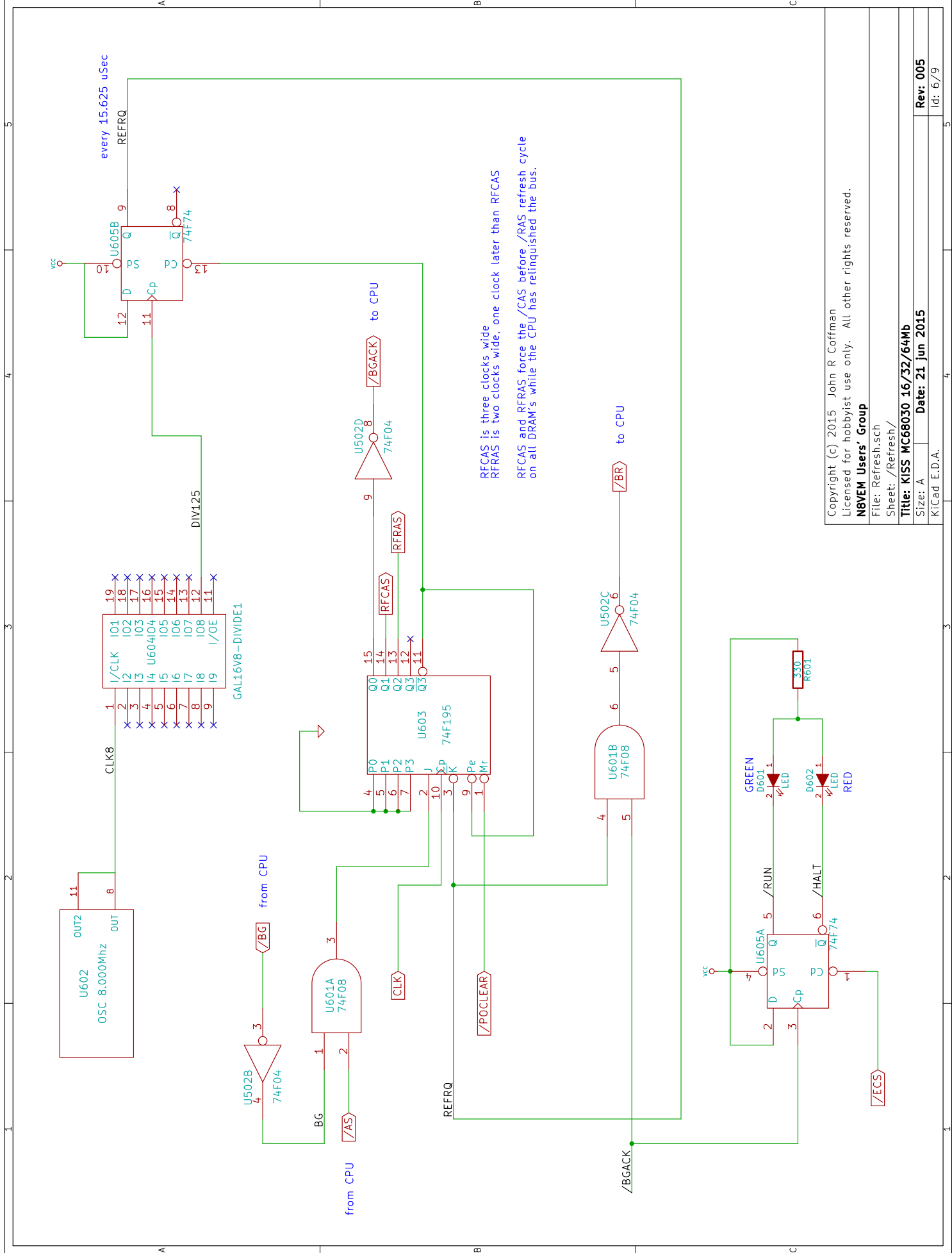
GAL22V10-HIGH9

GAL22V10-DRAM9

GAL22V10-BYTES9

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**N8VEM Users' Group**  
 File: DRcntrl.sch  
**Title: KISS MC68030 16/32/64Mb**  
 Size: A Date: 21 jun 2015  
 KiCad E.D.A.





REFREQ is three clocks wide  
 RFRAS is two clocks wide, one clock later than RFCAS  
 RFCAS and RFRAS force the /CAS before /RAS refresh cycle  
 on all DRAM's while the CPU has relinquished the bus.

