Retro-Brew Computing

ECB Prototype III with I/O Decode

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Overview

This is a new version of the prototyping board for new peripherals on the Z80 ECB bus. I/O decoding corrects the error on previous boards which do not take the /M1 signal into account (it must be high). The I/O decode is no longer on 4 high bits, but may be varied from 1 to 6 bits.

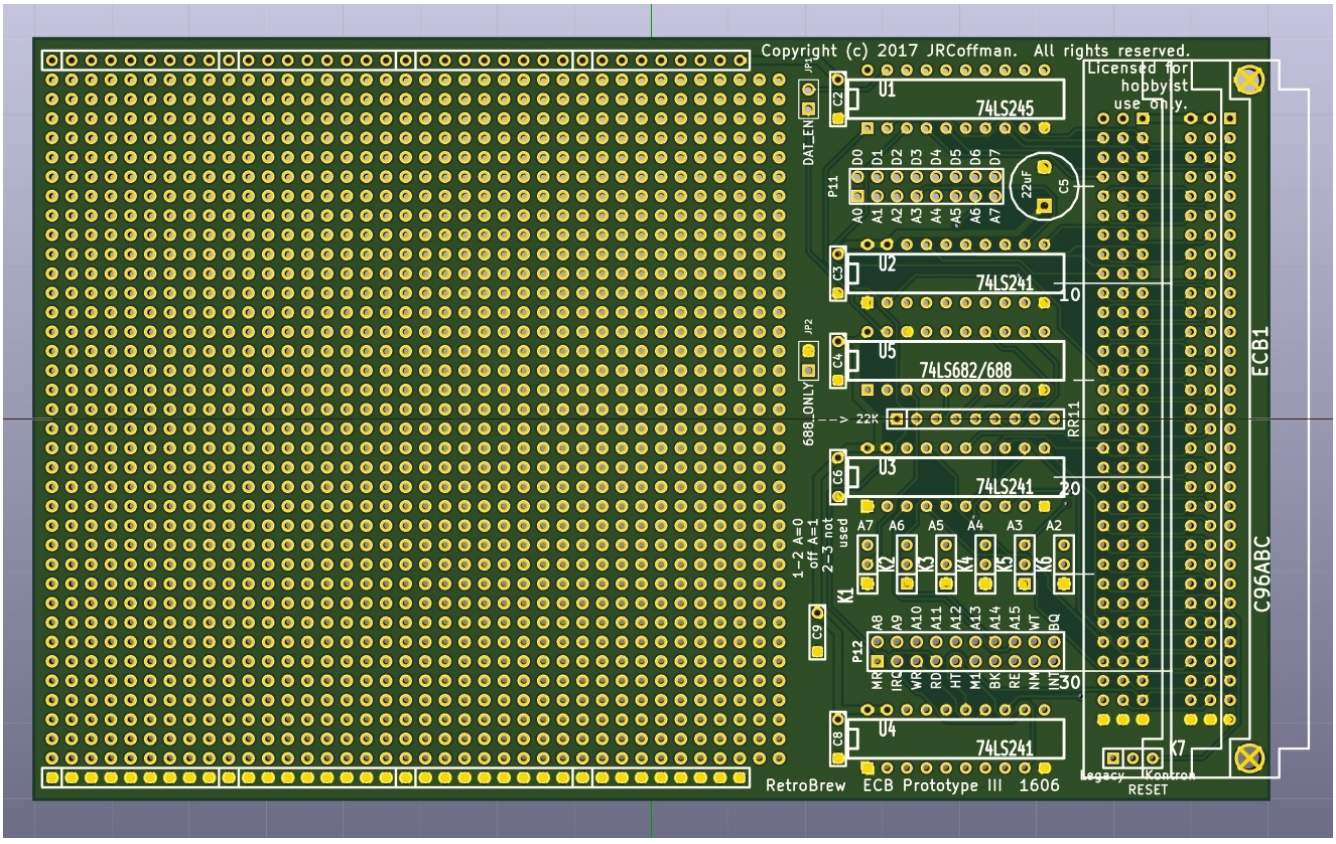

Figure 1. Board top view; unpopulated.

Description

The board plugs into the RetroBrew ECB backplane with the 96-pin right angle connector (ECB1), often an AMP 650913-? connector. All of the bus signals are duplicated on the 3x32 pin row, ECB2. K7 is the selector for N8 legacy RESET connection (RESET in on pin C31), or Kontron RESET connection (RESET in on pin C26. The Kontron connection is used by boards produced in the last 4 years, and is supported on the 12-slot Backplane (6508) and newest 8-slot Backplane-167.

Address selection is jumpered with K1..K6, which select the bit setting for the

address range A7..A2 which the board will respond to. If K? is left open, then the board will only respond when that bit is 1 (high). If K? is shorted 1-2 (pin 1 is square), then the board will only respond when that bit is 0 (low). If K? Is shorted 2-3, then that bit is ignored. Example: to prototype a -550 type UART, which has 8 internal registers, A7..A3 will be designated, and A2 will be set to “ingore”. The A2, A1, A0 will be connected to the corresponding address pins on the UART. Board selection will depend on A7..A3; i.e., the board will select on 8 I/O addresses.

Example: board to respond to the I/O address range 0xC0 to 0xC7.

K1	A7	open	1	
K2	A6	open	1	
K3	A5	1-2	0	
K4	A4	1-2	0	
K5	A3	1-2	0	
K6	A2	2-3	-	not decoded

A2,A1,A0 (P11 1,2,3) connected to UART address inputs

The board will select when /IORQ is low, /M1 is high and A7..A0 are B'1100_0xxx'. JP1 must be shorted to enable the 74LS245 data transceiver.

Note: The top layer of the board is filled with a ground (GND) plane; the bottom layer of the board is filled with a power (VCC) plane. Both planes are covered with solder mask, so shorting to one of the planes should not be an issue unless the board is drilled.

Chip Option 682/684/688

Either a 74LS682, 74LS684, or a 74LS688 chip may be used for the I/O decoding. The differences between these chips are fairly minor. The LS682 has internal pull-up resistors, and pin 1 is an output. The LS684 is the same pinout, but without the pull-up resistors. The LS688 lacks the pull-up resistors, and pin 1 is an enable input.

74LS682 – omit both JP2 and RR11 (22k SIP).
74LS684 – omit JP2, install RR11.
74LS688 – install both JP2 and RR11.

Logic Family

The circuitry is designed for 74LS logic only. These chips have hysteresis on the inputs and are, hence, more noise immune than any other logic family. The use of HC or HCT logic is discouraged.

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