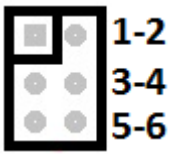
N8-2511 Jumper Settings
Oct-6-2011
Neil Breeden II

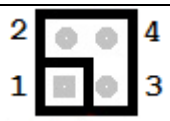
Notes:

- Reference the "N8-2511 – Jumper Locations" document for orientation and position of the jumpers on the printer circuit board.
- Defaults are provided only where they are applicable.
- Jumpers without defaults are dependent on the end users configuration.
-  Indicates that no jumper is used.
-  The orange line indicates that a jumper is to be used.
-  Is always Pin 1 in the jumper block (applies to 3 or more pin blocks).

P22	**Jumpers to allow setting of the internal I/O block of ports.**	
(Default)	1-2 3-4 5-6 Block Selected Base Port --- --- --- ---------- --------- OFF OFF OFF XXX111YY $E0-$FF $E0 OFF OFF ON XXX110YY $C0-$DF $C0 OFF ON OFF XXX101YY $A0-$BF $A0 OFF ON ON XXX100YY $80-$9F $80 ON OFF OFF XXX011YY $60-$7F $60 ON OFF ON XXX010YY $40-$5F $40 ON ON OFF XXX001YY $20-$3F $20 ON ON ON XXX000YY $00-$1F $00	
	With the default setting above the CSs are mapped as: /CS_PPI1 $80-$83 /CS_PPI2 $84-$87 /CS_RTC $88-$8B /CS_FDC $8C-$8F /CS_UTIL $90-$93 /ARCCS $94-$97 /VDPCS $98-$9B <- VDP at block $98-$9B /SNDCS $9C-$9F VDP at $98-$9B is done for MSX Compatibility.	P22 using default settings: 

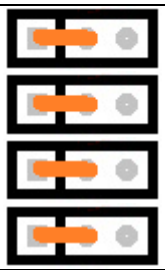
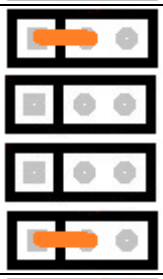
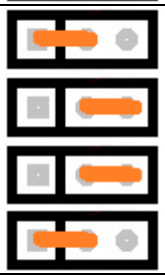
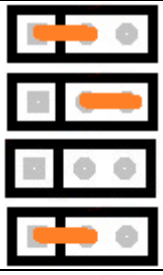
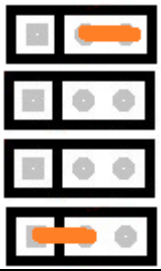
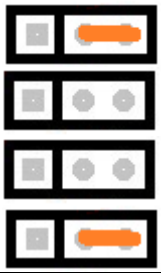
P22 Port to Device I/O Mapping

Device	Port	CPM Port	Port Read	Port Write	Function
/CS_PPI1	BASE BASE+1 BASE+2 BASE+3	$80 $81 $82 $83	Read Port A Read Port B Read Port C Read Control Byte	Write Port A Write Port B Write Port C Write Control Byte	Printer, Keyboard and Mouse
/CS_PPI2	BASE+4 BASE+5 BASE+6 BASE+7	$84 $85 $86 $87	Read Port A Read Port B Read Port C Read Control Byte	Write Port A Write Port B Write Port C Write Control Byte	General purpose parallel I/O
/CS_RTC	BASE+8 BASE+9 BASE+10 BASE+11	$88 $89 $8A $8B	Read from RTC N/U N/U N/U	Write to RTC N/U N/U N/U	Real Time Clock
/CS_FDC	BASE+12 BASE+13 BASE+14 BASE+15	$8C $8D $8E $8F	Read FDC Info Read FDC Status N/U N/U	Illegal (N/U) Write FDC Control N/U N/U	Floppy Disk Controller WDC37C65
/CS_UTIL	BASE+16 BASE+17 BASE+18 BASE+19	$90 $91 $92 $93	N/U N/U N/U N/U	/DACK /LDCR /LDOR /DACK and TC	Floppy Disk Controller WDC37C65
/ARCCS	BASE+20 BASE+21 BASE+22 BASE+23	$94 $95 $96 $97	N/U N/U N/U N/U	Various Enables N/U ROM A15...A19 N/U	Auxiliary Control Register
/VDPCS	BASE+24 BASE+25 BASE+26 BASE+27	$98 $99 $9A $9B	Read from VRAM Read VDP Register N/U N/U	Write to VRAM Write VDP Register N/U N/U	Video TMS9918
/SNDCS	BASE+28 BASE+29 BASE+30 BASE+31	$9C $9D $9E $9F	N/U DTB (Read from PSG) N/U N/U	DWS (Write to PSG) INTAK (Latch Address) N/U N/U	Sound AY-3-8910

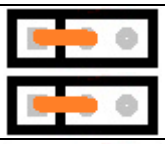
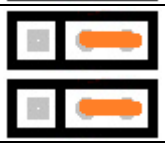
P43	Mono / Stereo Jumpers	
Stereo **(Default)**	1-2 Open 3-4 Open	
Mono	1-2 Connected 3-4 Connected	

P50	Interrupt Select	
Default:	1-2 Connected: /INT0 = /INT 3-4 Connected: /INT1 = /VINT	
Alternative:	1-3 Connected: /INT1 = /INT 2-4 Connected: /INT0 = /VINT	

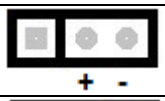
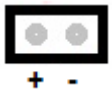
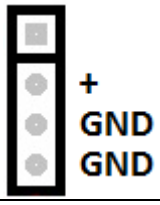
Note: The CP/M image requires an 8MB device such as the 27C080 EPROM.

K3,K4,K5,K18	**ROM Size**	
32 PIN-27C080 EPROM (Confirmed working)	K3: 1-2 K4: 1-2 K5: 1-2 K18: 1-2	
32 PIN-27C2001 EPROM (Confirmed working) K4 and K5 are not used.	K3: 1-2 K4: No Jumper K5: No Jumper K18: 1-2	
32-Pin 29x040 FLASH (Confirmed working)	K3: 1-2 K4: 2-3 K5: 2-3 K18: 1-2	
32-Pin 29x020 FLASH (Confirmed working) K5 is not used.	K3: 1-2 K4: 2-3 K5: No Jumper K18: 1-2	
28-Pin 27C512 Uses lower 28 Pins of the 32 pin socket. K4 and K5 are not used.	K3: 2-3 K4: No Jumper K5: No Jumper K18: 1-2	
28-Pin 27C256, 27C128, 27C64 Uses lower 28 Pins of the 32 pin socket. K4 and K5 are not used.	K3: 2-3 K4: No Jumper K5: No Jumper K18: 2-3	

K2	**Parallel I/O Port PIN 20**	
VSS	K2: 1-2	
VCC	K2: 2-3	

K9,K16	**RAM Size**	
512K SRAM (Confirmed working)	K9: 1-2 K16: 1-2	
128K SRAM (Confirmed working)	K9: 2-3 K16: 2-3	

K17	**Z8S180 Clock Source**	
VRY Clock	1-2	
P37 CPU Clock Frequency	2-3	

K19,P44,P45	SRAM Backup Battery	
K19	1-2 – SRAM backup power taken from backplane	
K19	2-3 – battery connector for external primary battery	
K19	Jumper 2-3 if no primary backup battery	
P44	Open – battery connector for external secondary backup battery	
P44	Installed - Jumper if no secondary backup battery	
P45	1-2 – RTC takes power from same source as SRAM	
P45	2 and 3 – Super CAP or Battery Backup for RTC Pin 2 is Positive Pin 3 and 4 are Negative	

The following configuration (no backup batteries) has been tested and works:

K19,P44,P45	No SRAM Backup Battery	
K19	Jumper 2-3 if no primary backup battery	
P44	Installed - Jumper if no secondary backup battery	
P45	1-2 – RTC takes power from same source as SRAM	

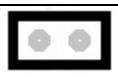
JP1	**JP1 ties to the SD so data can be read from the CPU on data bus (bit 6). This is optional in case SD is not installed and someone wants to use the input bit for something else.**	
Use Bit 6 for general input.	Open	
Use SD card	Installed	

JP7	**These allow the 8255 PPI to optionally use the interrupt modes for PC3. These won't help with IDE interrupts but could be used with the peripheral expansion port if needed.** Also, I think the IDE port interrupt could tie to these jumpers but it would require a wire jumper. More experimentation needed here.	
Disable interrupt modes **(Default)**.	Open	
Enable interrupt modes.	Installed	

JP8	**These allow the 8255 PPI to optionally use the interrupt modes for PC0. These won't help with IDE interrupts but could be used with the peripheral expansion port if needed.** Also, I think the IDE port interrupt could tie to these jumpers but it would require a wire jumper. More experimentation needed here.	
Disable interrupt modes **(Default)**.	Open	
Enable interrupt modes.	Installed	

JP10	**AY-3-8910 TEST2 PIN 26**	
Float (High)**(Default)**	Open	
VSS (low)	Installed	

JP11	**SD Socket Power Enable**	
No power to SD	Open	
3.3VDC to SD	Installed	

JP12	**Optionally allows the interrupt signal from the ECB into the internal interrupt circuitry. This supports interrupt prioritization of devices on the bus.**	
Disallow interrupt prioritization.	Open	
Allow interrupt prioritization.	Installed	

JP13	**IOA6 is on the AY-3-8910 and is potentially an unused input (depending on its configuration) so it can be optionally tied to ground to prevent it from floating. Also it provides a handy tie in to use this optional input pin.**	
Float IOA6 **(Default)**	Open	
Ground IOA6	Installed	

Change List:

7/16/2011 – Initial release
7/19/2011 – Updated the FLASH/EPROM jumpers (K3,K4,K5,K18) to be correct and to represent the various sizes.
– Added Backup battery polarities.
7/20/2011 – Updated the EPROM/FLASH grid to identify tested configurations and added new devices
– Added “No Backup Battery” configuration
– Added confirmation that the 512K and 128K SRAM jumpers work.
7/21/2011 – Corrected typo for 29F020
7/30/2011 – Added Port I/O Mapping info