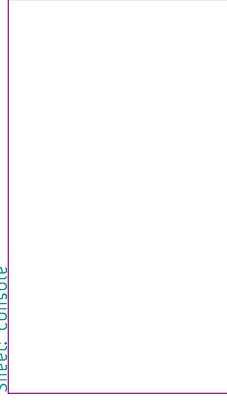


Sheet: console



File: console.sch

Sheet: cpu



File: cpu.sch

Sheet: ide



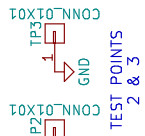
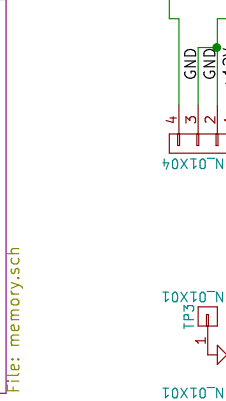
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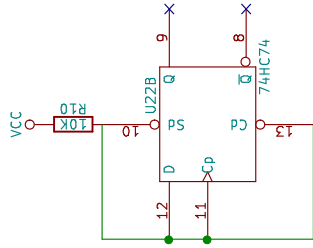
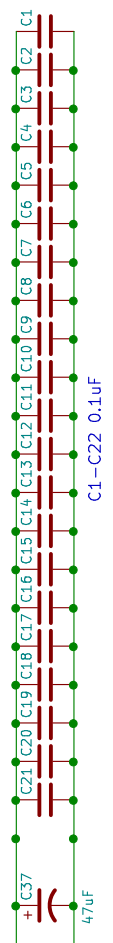
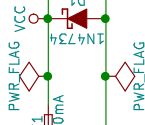


File: iot.sch

Sheet: memory



TEST POINTS
2 & 3



3.2MM MOUNTING HOLES

SPARETIMEGIZMOS
SPARE TIME GIZMOS LOGO
LOGO1

RBC EDITION V1.00 SCHEMATIC CHANGES FROM ORIGINAL STG SCHEMATIC:

1. RELOCATED POWER INPUT/DECOUPLING CAPS TO TOP LEVEL SHEET.
2. RELOCATED TP2/TP3 TO TOP LEVEL SHEET.
3. RELOCATED SPARE/JUNUSED 74HC74 TO TOP LEVEL SHEET.
4. CPU SHEET: /INTGNT MOVED FROM PIN 31 TO PIN 31 ON HD-6120 PER DATASHEET. DWAGNT MOVED FROM PIN 31 TO PIN 31 ON HD-6120 PER DATASHEET.
5. CPU SHEET: CHANGED TP1 TO J17 WITH A CONNECTION TO GROUND TO ALLOW AN OFF-BOARD RESET SWITCH TO BE USED.
6. MEMORY SHEET: CHANGED SRAM CHIPS FROM QTY. 3 4-BIT WIDTH CHIPS TO QTY. 2 8-BIT WIDTH CHIPS.
7. MEMORY SHEET: ADDED J15 TO ALLOW FOR 27C256 EPROMS OR 28C256 EEPROMS TO BE USED. WITH CORRESPONDING UPDATES TO SOCKET PIN ASSIGNMENTS.
8. IDE SHEET: ADDED F2, J16 & C22 TO ALLOW POWER TO BE SUPPLIED TO CF -> IDE ADAPTERS.

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Sheet: /
 File: SBC6120-RBC.sch

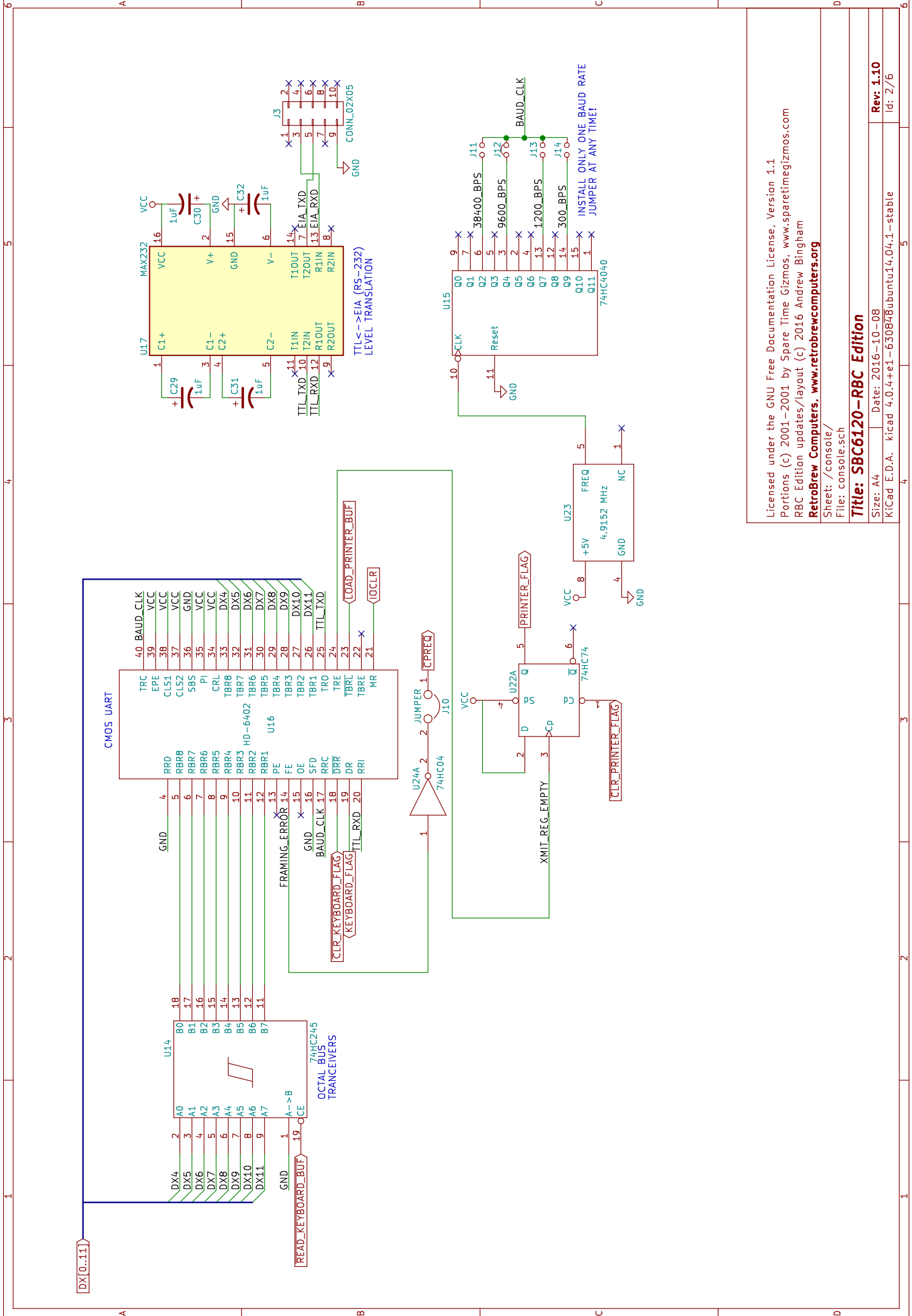
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Size: A4 | Date: 2016-10-08

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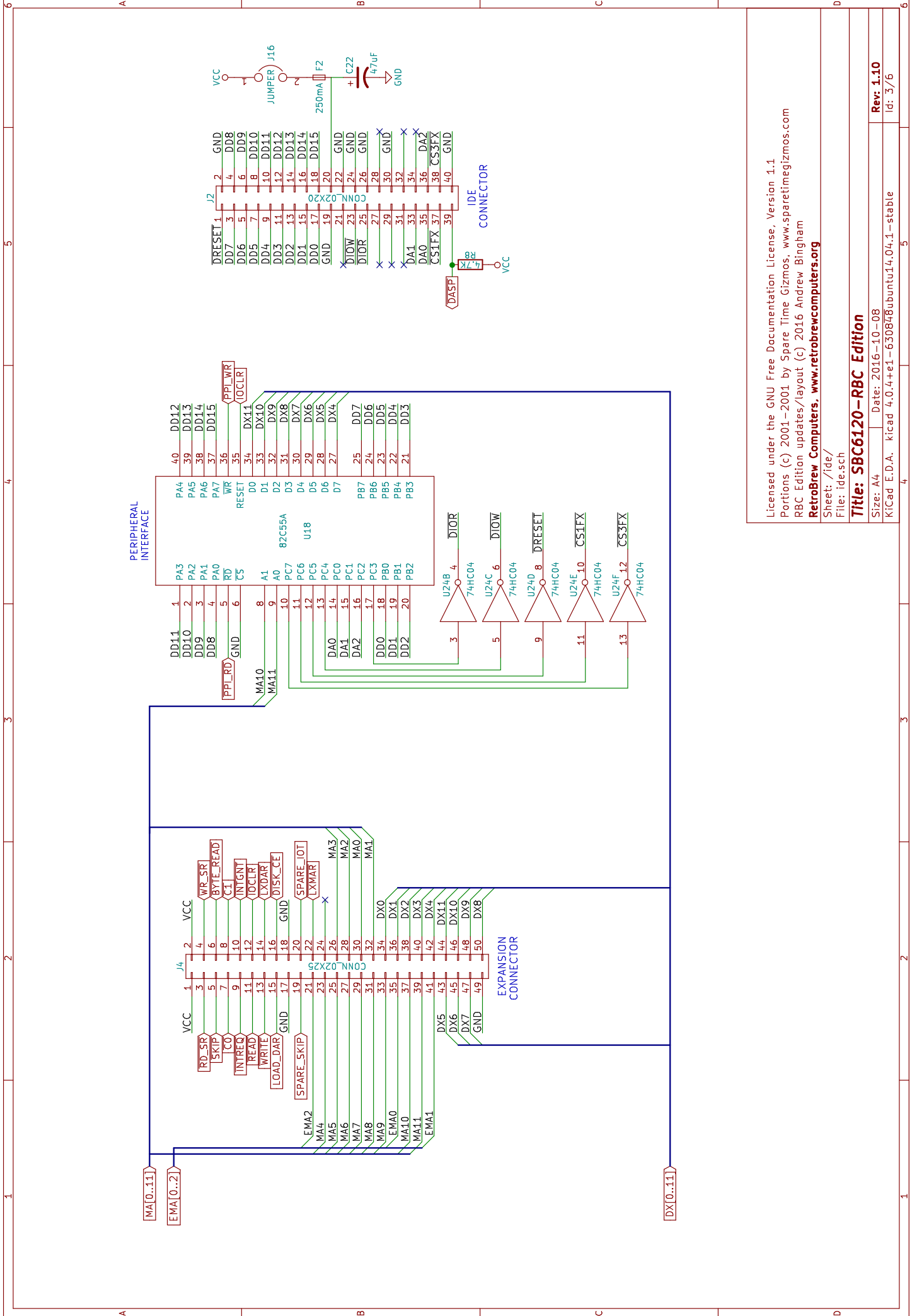
Rev: 1.10

Id: 1/6



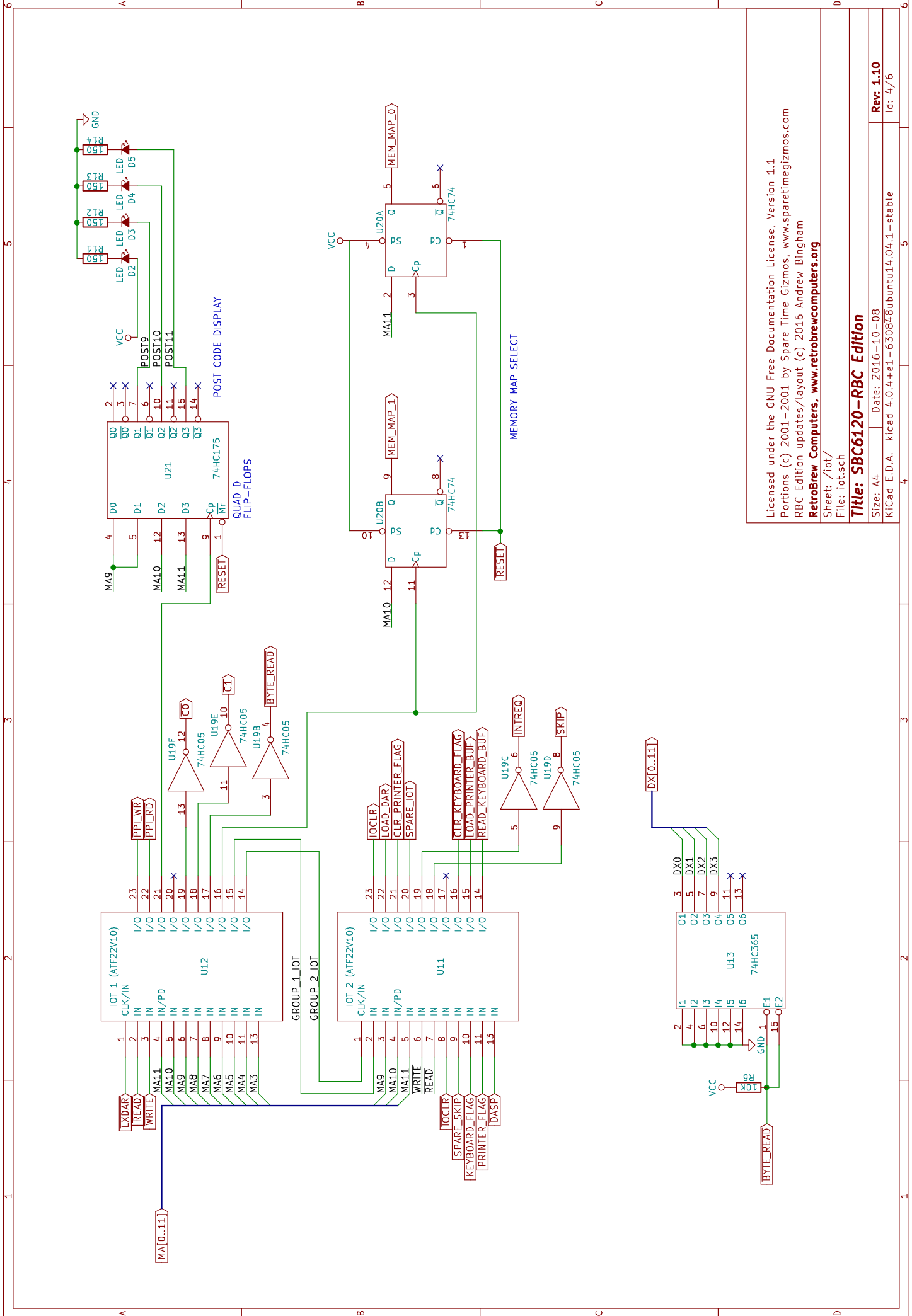
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 File: console.sch

Title: SBC6120-RBC Edition
 Size: A4 | Date: 2016-10-08
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 Sheet: /Ide/
 File: ide.sch

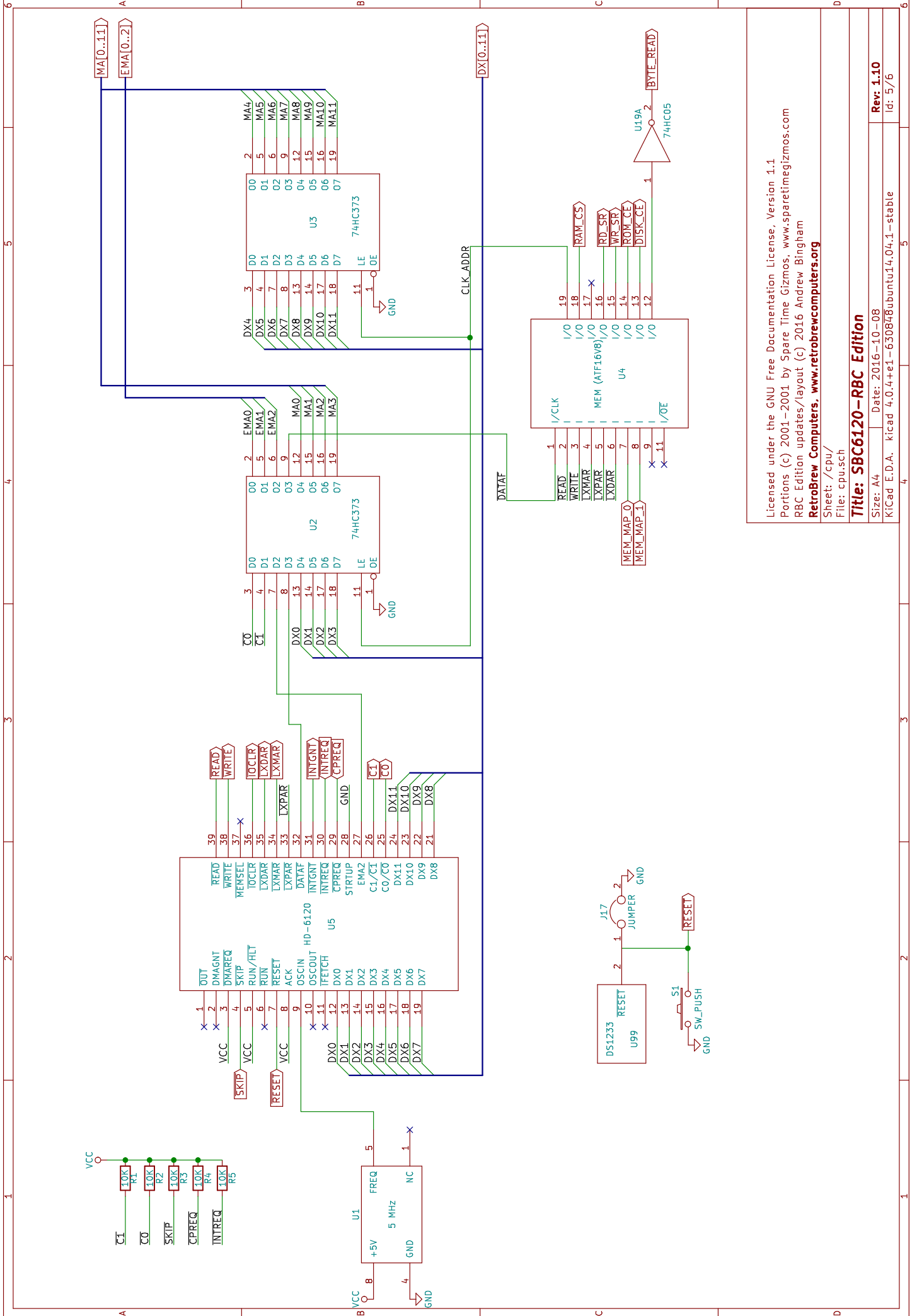
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 File: iot.sch

Title: SBC6120-RBC Edition

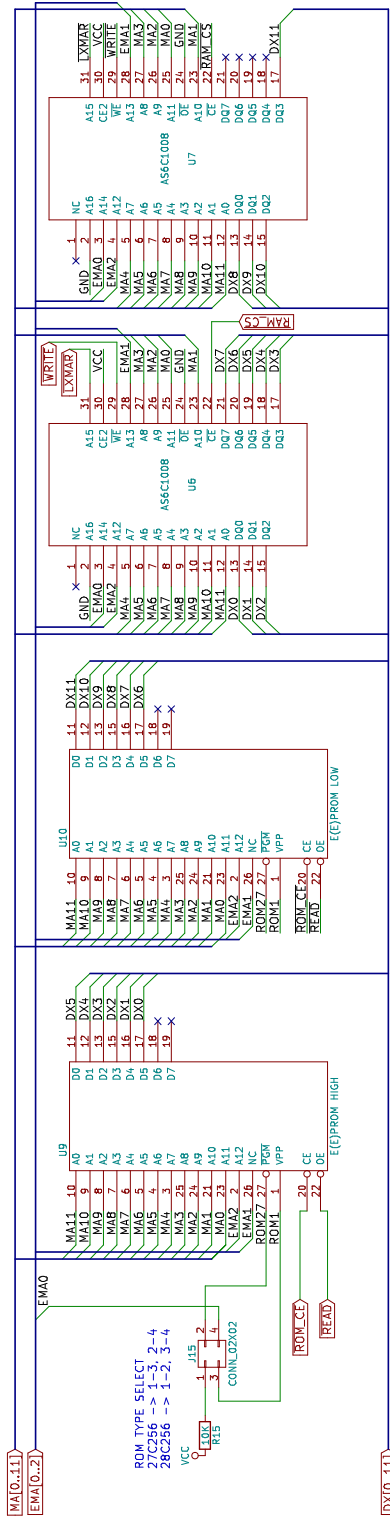
Size: A4 | Date: 2016-10-08 | Rev: 1.10
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 Sheet: /cpu/
 File: cpu.sch

Title: SBC6120-RBC Edition

Size: A4 | Date: 2016-10-08 | **Rev. 1.10**
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 Sheet: /memory/
 File: memory.sch
Title: SBC6120-RBC Edition
 Size: A3 Date: 2016-10-08 Rev: 1.10
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