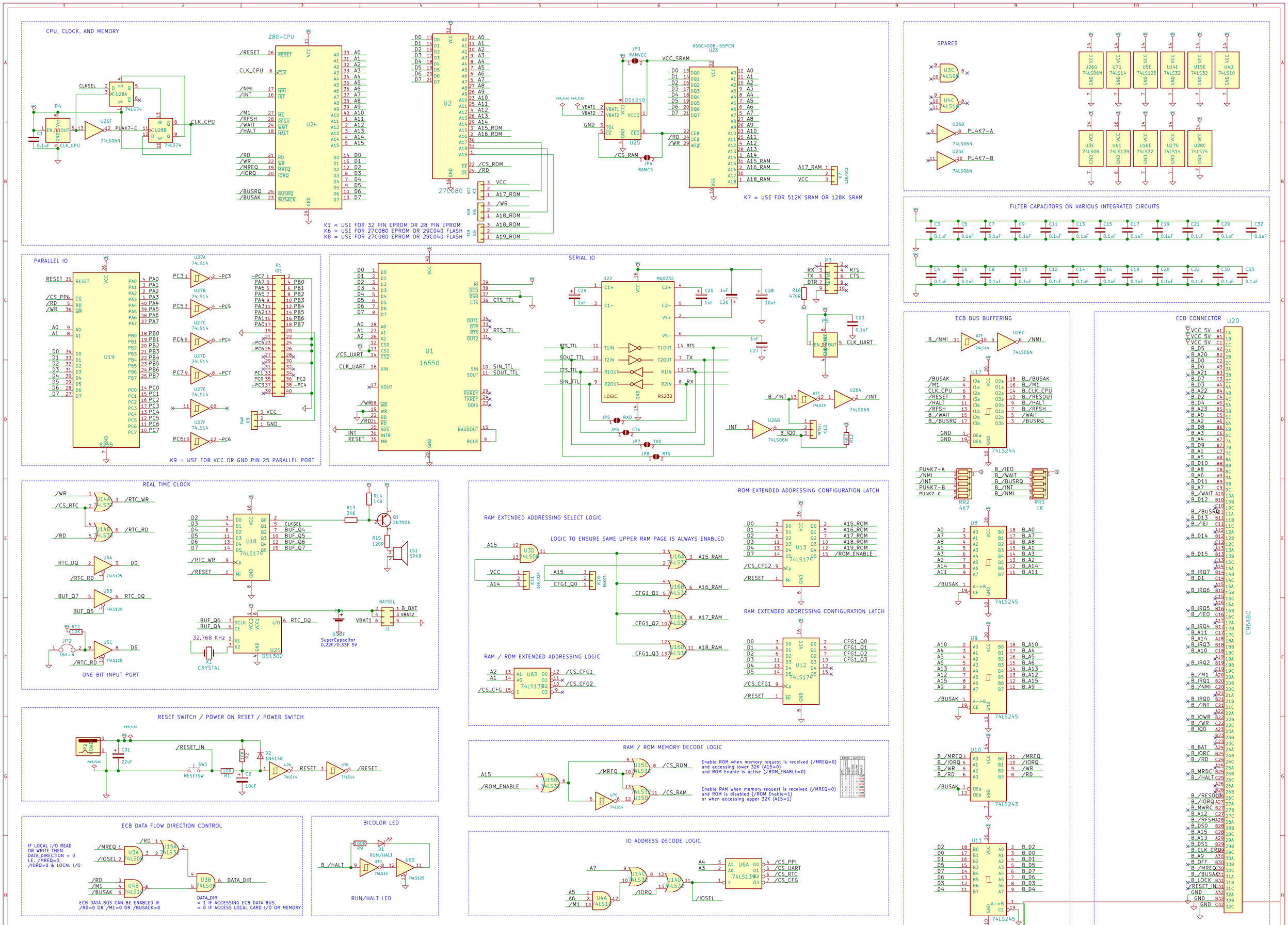
CPU, CLOCK, AND MEMORY
Z80-CPU
U24
U2
27C080
AS6C4008-55PCN
U23
DS1210
U25
K1 = USE FOR 32 PIN EPROM OR 28 PIN EPROM
K6 = USE FOR 27C080 EPROM OR 29C040 FLASH
K8 = USE FOR 27C080 EPROM OR 29C040 FLASH
K7 = USE FOR 512K SRAM OR 128K SRAM
SPARES
FILTER CAPACITORS ON VARIOUS INTEGRATED CIRCUITS
PARALLEL IO
U19
8255
K9 = USE FOR VCC OR GND PIN 25 PARALLEL PORT
SERIAL IO
U1
16550
U22
MAX232
ECB BUS BUFFERING
U17
74LS244
ECB CONNECTOR
U20
C96ABC
REAL TIME CLOCK
U18
74LS174
U21
DS1302
ONE BIT INPUT PORT
RAM EXTENDED ADDRESSING SELECT LOGIC
LOGIC TO ENSURE SAME UPPER RAM PAGE IS ALWAYS ENABLED
ROM EXTENDED ADDRESSING CONFIGURATION LATCH
RAM EXTENDED ADDRESSING CONFIGURATION LATCH
RAM / ROM EXTENDED ADDRESSING LOGIC
RAM / ROM MEMORY DECODE LOGIC
Enable ROM when memory request is received (/MREQ=0) and accessing lower 32K (A15=0) and ROM Enable is active (/ROM_ENABLE=0)
Enable RAM when memory request is received (/MREQ=0) and ROM is disabled (/ROM Enable=1) or when accessing upper 32K (A15=1)
IO ADDRESS DECODE LOGIC
RESET SWITCH / POWER ON RESET / POWER SWITCH
ECB DATA FLOW DIRECTION CONTROL
IF LOCAL I/O READ OR WRITE THEN DATA_DIRECTION = 0 I.E. /MREQ=0, /IORQ=0 & LOCAL I/O
ECB DATA BUS CAN BE ENABLED IF /RD=0 OR /M1=0 OR /BUSACK=0
DATA_DIR = 1 IF ACCESSING ECB DATA BUS, = 0 IF ACCESS LOCAL CARD I/O OR MEMORY
BICOLOR LED
RUN/HALT LED
Sheet: /
File: SBC.sch
Title:
Size: C
Date: 2019-06-21
Rev:
KiCad E.D.A. kicad (5.1.4)-1
Id: 1/1