RF1: latch in the output of refresh timer, waiting for negation of AS
RF2: start of the refresh cycle
RF2.5: CAS asserts at the falling edge of clock
RF3: RAS asserts for 2 clocks

OUTPUT   RefreshRAS

make sure there are enough time for RAS precharge after the refresh is done
hold off dtack until refresh finished
start the refresh when nAS is high

OUTPUT   RF1

OUTPUT   RF2

refresh

count256

ras refresh
RF3

up counter

nRESET   INPUT   NOT   sclr   q[7..0]   cout
                        VCC   inst58   clock

inst33

CLK

SRFF   RF1   AND2   SRFF   RF2   AND2   DFF   AND2   DFF   NOT
PRN   PRN   PRN   PRN
S   Q   inst65   S   Q   inst72   D   Q   inst73   D   Q   inst74
R   CLRN   R   CLRN   CLRN   CLRN
inst66   inst69   inst59   inst60

nRESET   CLK   CLK   CLK

nAS   INPUT   nAS
        VCC

CLK   INPUT   NOT   nCLK
        VCC   inst

cas refresh
DFFE   RF2.5
PRN
nCLK   D   Q
        ENA
        CLRN   OUTPUT   RefreshCAS
inst83