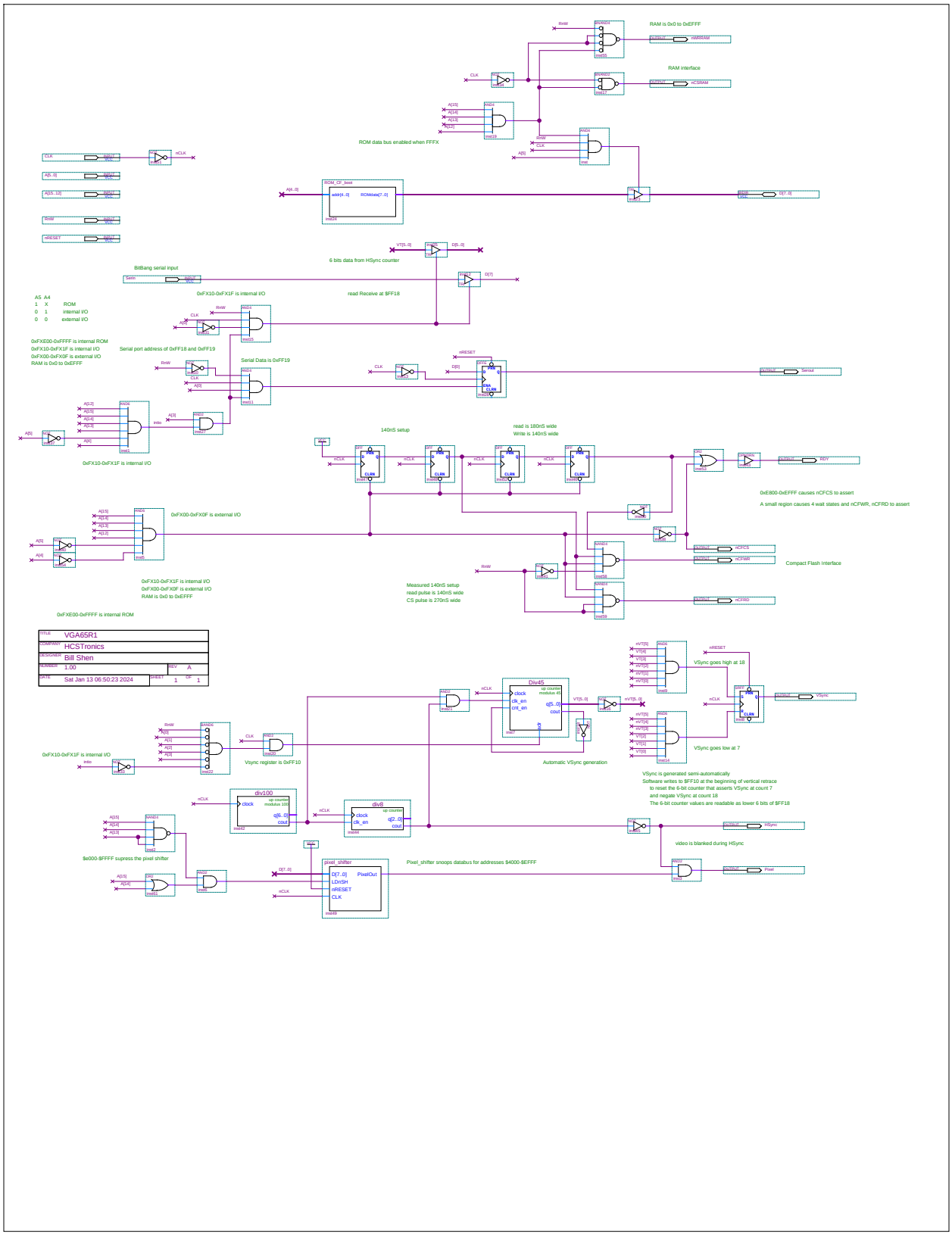
RAM is 0x0 to 0xEFFF
RAM interface
ROM data bus enabled when FFFX
6 bits data from HSync counter
BitBang serial input
read Receive at $FF18
0xFX10-0xFX1F is internal I/O
A5 A4
1 X ROM
0 1 internal I/O
0 0 external I/O
0xFXE00-0xFFFF is internal ROM
0xFX10-0xFX1F is internal I/O
0xFX00-0xFX0F is external I/O
RAM is 0x0 to 0xEFFF
Serial port address of 0xFF18 and 0xFF19
Serial Data is 0xFF19
140nS setup
read is 180nS wide
Write is 140nS wide
0xE800-0xEFFF causes nCFCS to assert
A small region causes 4 wait states and nCFWR, nCFRD to assert
Compact Flash Interface
Measured 140nS setup
read pulse is 140nS wide
CS pulse is 270nS wide
TITLE VGA65R1
COMPANY HCSTronics
DESIGNER Bill Shen
NUMBER 1.00
REV A
DATE Sat Jan 13 06:50:23 2024
SHEET 1 OF 1
VSync goes high at 18
VSync goes low at 7
Automatic VSync generation
Vsync registar is 0xFF10
VSync is generated semi-automatically
Software writes to $FF10 at the beginning of vertical retrace
to reset the 6-bit counter that asserts VSync at count 7
and negate VSync at count 18
The 6-bit counter values are readable as lower 6 bits of $FF18
video is blanked during HSync
$e000-$FFFF supress the pixel shifter
Pixel_shifter snoops databus for addresses $4000-$EFFF
Div45
div100
div8
pixel_shifter