TS16M3260N

64MB 72 PIN FPM
DRAM SIMM With 16Mx4 5VOLT

Description

The TS16M3260N is a 16M by 32-bit dynamic RAM module with 8 pcs of 16Mx4 DRAMs assembled on the printed circuit board.

The TS16M3260N is optimized for application to systems which require high density and large capacity along with compact sizing.

Features

- 16,777,216 word by 32-bit organization.
- Fast Page Mode operation.
- Single +5.0V ± 10% power supply.
- 4,096 cycles refresh.
- Lower power consumption.
- CAS before RAS refresh, RAS only refresh, Hidden refresh, Fast Page Mode, Read_Modify_Write capability.

TS16M3260N	
Access time from /RAS t_{RAC}	60ns
Access time from /CAS t_{CAC}	15ns
Random read/write cycle Time t_{RC}	110ns
Page mode cycle time t_{PC}	40ns

Dimensions

Side	Millimeters	Inches
A	107.95 ± 0.40	4.250 ± 0.016
B	6.35	0.250
C	3.38	0.133
D	2.03	0.008
E	26.00 ± 0.20	1.020± 0.008
F	10.16	0.400
G	6.35	0.250
H	1.27 ± 0.10	0.050 ± 0.004

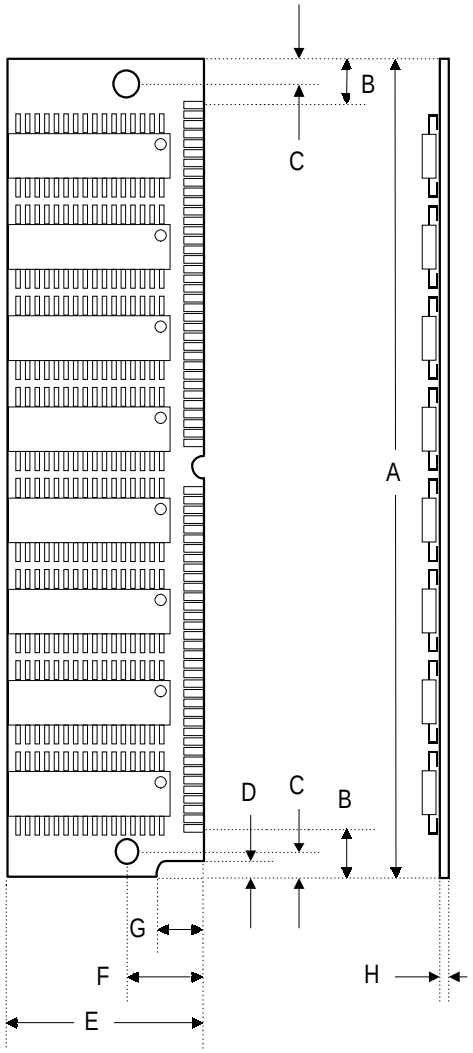
(Refer Placement)

Pin Identification

Symbol	Function
A0~A11	System Address inputs
D0 ~ D31	Common data inputs/outputs
/RAS0,/RAS2	System Row address strobes
/CAS0~/CAS3	System column address strobes
/WE	System Write enable
Vss	Ground
Vcc	+5 voltage power supply
NC	No Connection
PD1~PD4	Presence detection pin

(Refer Block Diagram)

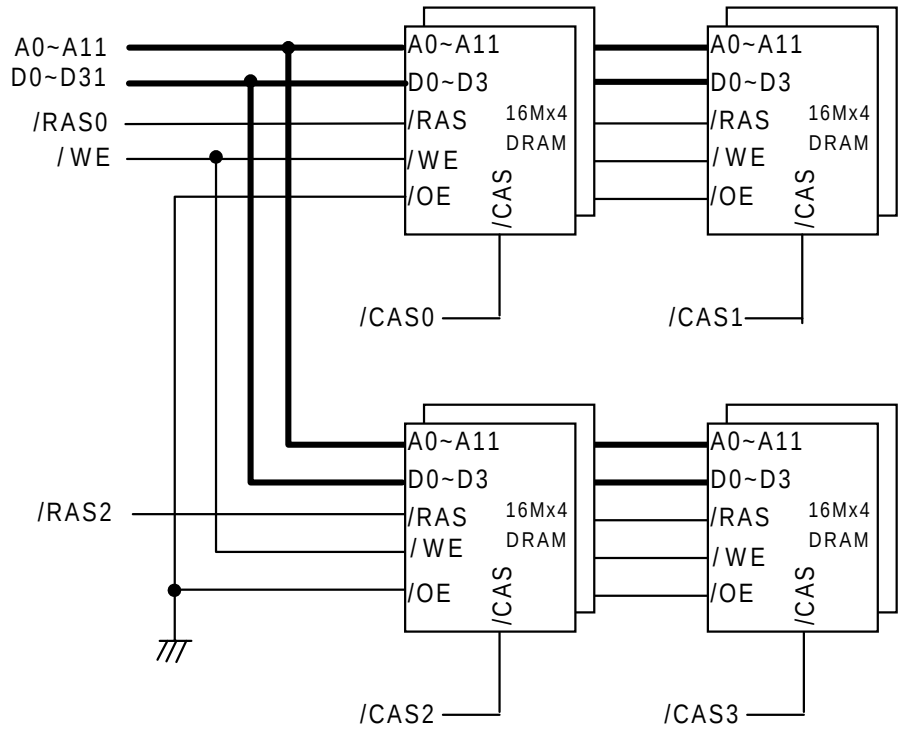
Placement:



Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	Vss	13	A1	25	D22	37	NC	49	D8	61	D13
02	D0	14	A2	26	D7	38	NC	50	D24	62	D30
03	D16	15	A3	27	D23	39	Vss	51	D9	63	D14
04	D1	16	A4	28	A7	40	/CAS0	52	D25	64	D31
05	D17	17	A5	29	A11	41	/CAS2	53	D10	65	D15
06	D2	18	A6	30	Vcc	42	/CAS3	54	D26	66	NC
07	D18	19	A10	31	A8	43	/CAS1	55	D11	67	PD1
08	D3	20	D4	32	A9	44	/RAS0	56	D27	68	PD2
09	D19	21	D20	33	NC	45	NC	57	D12	69	PD3
10	Vcc	22	D5	34	/RAS2	46	NC	58	D28	70	PD4
11	NC	23	D21	35	NC	47	/WE	59	Vcc	71	NC
12	A0	24	D6	36	NC	48	NC	60	D29	72	Vss

TS16M3260N-- Block Diagram



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{cc} supply relative to Vss	V_{cc}	-1 to +7.0	V
Storage temperature	T_{stg}	-55 to +125	°C
Power dissipation	P_D	8	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.
Exposure to absolute maximum rating conditions for intended periods may affect device reliablilty.

RECOMMENDED OPERATION CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	V_{ss}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc[*1]	V
Input Low Voltage	V_{IL}	-1.0[*2]	-	0.8	V

Note: *1: Vcc +2.0V at pulse width≦20s, witch is measured at Vcc.

*2: -2.0V at pulse width≦20ns, witch is measured at Vss.

DC AND OPERATION CHARACTERISTICS (Recommended operationg conditions unless otherwise noted)

Symbol	Min	Max	Unit
I_{CC1}	-	880	mA
I_{CC2}	-	16	mA
I_{CC3}	-	880	mA
I_{CC4}	-	480	mA
I_{CC5}	-	8	mA
I_{CC6}	-	880	mA
$I_{I(L)}$	-10	10	uA
$I_{O(L)}$	-5	5	uA
V_{OH}	2.4	-	V
V_{OL}	-	0.4	V

I_{CC1}: Operation Current* (/RAS, /CAS, Address cycling @t_{RC}=min)
I_{CC2}: Standby Current (/RAS=/CAS=/W=V_{IH})
I_{CC3}: /RAS Only Refresh Current* (/CAS=V_{IH}, /RAS cycling @t_{RC}=min)
I_{CC4}: Fast Page Mode Current* (/RAS=V_{IL}, /CAS cycling: t_{PC}=min)
I_{CC5}: Standby Current (/RAS=/CAS=/W=Vcc-0.2V)
I_{CC6}: /CAS-Before-/RAS Refresh Current* (/RAS and /CAS cycling @t_{RC}=min)
$I_{(IL)}$: Input Leakage Current (Any input $0 \leqq V_{IN} \leqq$ Vcc+0.5V, all other pins not under test=0 V)
$I_{(OL)}$: Output Leakage Current (Data Out is disabled, $0V \leqq V_{OUT} \leqq$ Vcc)
V_{OH}: Output High Voltage Level (I_{OH} = -5mA)
V_{OL}: Output Low Voltage Level (I_{OL} = 4.2mA)

***Note:** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once while /RAS= V_{IL}.. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (TA = 25°C, Vcc = 5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance (A0~A11)	C_{IN1}	-	50	pF
Input capacitance (/WE)	C_{IN2}	-	66	pF
Input capacitance (/RAS0, /RAS2)	C_{IN3}	-	38	pF
Input capacitance (/CAS0~/CAS3)	C_{IN4}	-	24	pF
Data input/output capacitance (D0~D31)	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0℃ ≦TA≦70℃, Vcc=5.0V±10%, See notes 1, 2)

Test condition: Vih/Vil=2.4/0.8V, Voh/Vol=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	Min	Max	Unit	Note
Random read or write cycle time	t_{RC}	110		ns	
Access time from /RAS	t_{RAC}		60	ns	3,4,10
Access time from /CAS	t_{CAC}		15	ns	3,4,5
Access time from column address	t_{AA}		30	ns	3,10
/CAS to output in Low-Z	t_{CLZ}	0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	ns	6

Transition time(rise and fall)	t_T	1	50	ns	2
/RAS precharge time	t_{RP}	40		ns	
/RAS pulse width	t_{RAS}	60	10K	ns	
/RAS hold time	t_{RSH}	15		ns	

AC CHARACTERISTICS (0℃≦TA≦70℃, Vcc=5.0V±10%, See notes 1, 2)

Test condition: Vih/Vil=2.4/0.8V, Voh/Vol=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	Min	Max	Unit	Note
/CAS hold time	t_{CSH}	60		ns	
/CAS pulse width	t_{CAS}	15	10K	ns	
/RAS to /CAS delay time	t_{RCD}	20	45	ns	4
/RAS to column address delay time	t_{RAD}	15	30	ns	10
/CAS to /RAS precharge time	t_{CRP}	5		ns	
Row address set-up time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	10		ns	
Column address set-up time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	10		ns	
Column address to /RAS lead time	t_{RAL}	30		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold referenced to /CAS	t_{RCH}	0		ns	8
Read command hold referenced to /RAS	t_{RRH}	0		ns	8
Write command hold time	t_{WCH}	10		ns	
Write command pulse width	t_{WP}	10		ns	
Write command to /RAS lead time	t_{RWL}	15		ns	
Write command to /CAS lead time	t_{CWL}	15		ns	
Date set-up time	t_{DS}	0		ns	9
Date hold time	t_{DH}	10		ns	9
Refresh period	t_{REF}		64	ms	
Write command set-up time	t_{WCS}	0		ns	7
/CAS setup time(/CAS-before-/RAS refresh)	t_{CSR}	5		ns	
/CAS hold time (/CAS-before-/RAS refresh)	t_{CHR}	10		ns	
/RAS to /CAS precharge time	t_{RPC}	5		ns	

Access time from /CAS precharge	t_{CPA}		35	ns	3
Fast page mode cycle time	t_{PC}	40		ns	
/CAS precharge time (Fast page cycle)	t_{CP}	10		ns	
/RAS pulse width (Fast page cycle)	t_{RASP}	60	200K	ns	
/W to /RAS precharge time (C-B-R refresh)	t_{WRP}	10		ns	
/W to /RAS hold time (C-B-R refresh)	t_{WRH}	10		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH}/V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geqq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the /CAS leading edge in early write cycle.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.